REMARKS

Claims 1-16 are pending. Claims 1-16 were rejected by the Examiner in the Office Action dated October 29, 2008. Reconsideration of all rejected claims is requested in light of the arguments and amendments presented here.

Claim Rejections Under 35 U.S.C. §112

Claims 1-14 and 16 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite because of lack of antecedent basis in claims 1 and 16. Claims 1 and 16 are amended appropriately. Therefore the rejection is overcome.

Claim Rejections Under 35 U.S.C. §102

Claims 1-3, 9, and 10 were rejected under 35 U.S.C. §102(b) as being anticipated by prior art disclosed in Figure 1 of the present application. While Figure 1 is not believed to be prior art under 35 USC 102(b) and thus provides no basis for the present rejection, this response is provided on the understanding that 35 USC 102(a) may provide such a basis, and that section 102(b) may have been cited in error.

Claim 1 recites, "the input line network is configured to provide at least a first one of the input signals to both a first K-LUT portion and a second K-LUT portion in a first state, and provide a first carry-in signal to the first K-LUT portion and a second carry-in signal to the second K-LUT portion in a second state." In contrast, Figure 1 shows only one carry-in signal C_{in} which can be provided to both K-LUT portions.

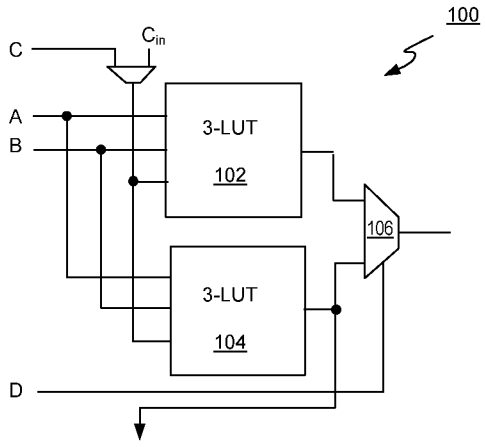


FIG. 1

The Office Action indicated that first and second carry-in signals are obtained from C_{in} in Figure 1. However, neither Figure 1 nor the related text disclose obtaining such first and second carry-in signals. The specification consistently refers to the carry-in of the previous stage. "Conventional implementations of LUT arithmetic use one 3-LUT of a 4-LUT to generate the sum from two summand signals and the carry_in of the previous stage. The other 3-LUT generates the carry_out of the stage from the same three input signals (i.e. the two summand signals and the carry_in of the previous stage). Paragraph 0003. This configuration is also shown in Figure 2. "Figure 2 is a block diagram of a LUT 200, illustrating the LUT 100 configured according to the conventional approach." Paragraph 0003.

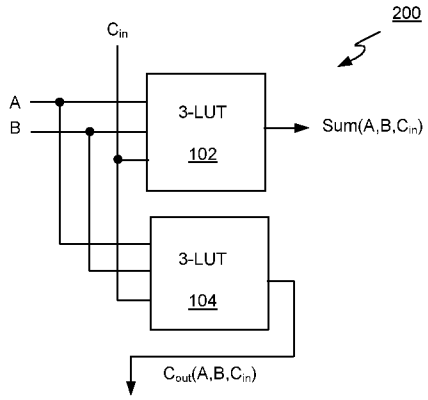


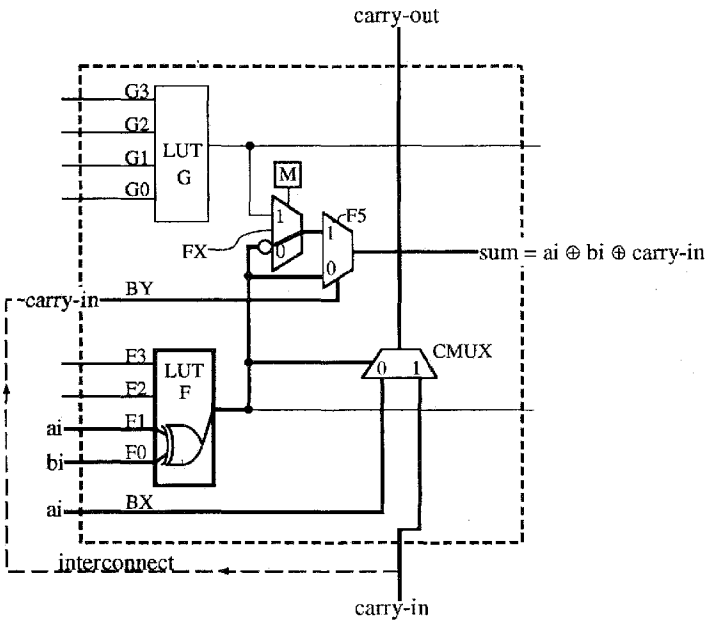
FIG. 2

Figure 2 shows C_{in} provided to both 3-LUT 102 and 3-LUT 104. Thus, providing a first carry-in signal to the first K-LUT portion and a second carry-in signal to the second K-LUT portion according to claim 1 is not shown. Therefore, claim 1 is allowable.

Claims 2-14 depend from claim 1 and are submitted to be allowable at least for depending from an allowable base claim. Furthermore, rejected claims 2, 3, 9, and 10 recite additional features that were not identified in the Office Action and thus provide additional reasons for allowance. For example, claim 10 recites, "the input multiplexers are configurable such that, in the first state, each of the input multiplexers provides the particular binary input signal to the output of that multiplexer and, in the second state, each of at least some of the input multiplexers provides other than the particular binary input signal to the output of that multiplexer." No features of Figure 1 were cited as corresponding to these features and Figure 1 shows only one input multiplexer.

Claim Rejections Under 35 U.S.C. §103

Claim 15 was rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,682,107 to Tavana et al. ("Tavana") in view of U.S. Patent No. 5,724,276 to Rose et al. ("Rose"). Claim 15 recites, "at least one output multiplexer, each of the at least one output multiplexers coupled to select among signals at the outputs of the K-LUT, under the control of a carry-in signal to the LE." The Office action cited multiplexer F5 of Figure 2b of Rose as showing these features. The Office action stated, "when M is set to 1, the MUX F5 clear [sic] select between the outputs of LUT G and LUT [F] as claimed," (emphasis added). However, Fig. 2b (reproduced below) shows an adder configuration in which M is set to 0. "FIG. 2b shows the structure of FIG. 2a implemented as a one bit of an adder (the function shown in FIG. 1b). Portions of the structure not used for the adder function are shown in faint lines and portions which implement the adder are shown in heavy lines." Column 2, lines 63-67. And in this configuration, multiplexer F5 selects between the output of LUT F and its inverse, not between signals at the outputs of a K-LUT.



ADDER BIT

Fig. 2b

Rose discloses that when M is set to 1, multiplexer F5 selects between outputs of LUT G and LUT F as in Fig. 1a. "If memory cell M carries a logic 1, the LUT G output signal is provided to multiplexer F5 and multiplexer F5 functions as in FIG. 1a." Column 2, lines 40-42. However, as shown in Fig. 1a, in this configuration multiplexer F5 is not controlled by a carry-in signal.

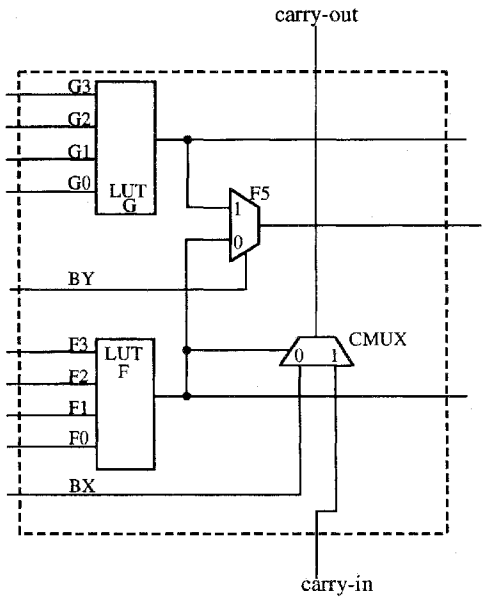


Fig. 1a

Prior Art

Thus, neither of the two configurations of memory cell M provides a multiplexer according to claim 15. In particular, if M is set to 1 as indicated in the Office action, then multiplexer F5 is not under the control of a carry-in signal.

Allowable Subject Matter

The only rejection stated with respect to claims 4-8, 11-14, and 16 was under 35 USC 112. Because this rejection is overcome, no rejection remains with respect to these claims. Therefore, an indication of allowability of these claims is requested.

Finality of Office Action

The Office Action of October 29, 2008 was indicated to be final. However, the finality of

the rejection is not proper. In particular, a new ground of rejection was introduced with respect to claims 1-3, 9, and 10, based on an amendment to claim 1. However, MPEP 706.07(a) states, "A second or any subsequent action on the merits in any application or patent involved in reexamination proceedings should not be made final if it includes a rejection, on prior art not of record, of any claim amended to include limitations which should reasonably have been expected to be claimed." Claim 1 was amended to include elements from claim 4 (indicated to be allowable), which should reasonably have been expected because this could also provide a basis for allowance of claim 1. Because the finality of the Office Action was premature, it should be withdrawn. "If, on request by applicant for reconsideration, the primary examiner finds the final rejection to have been premature, he or she should withdraw the finality of the rejection." MPEP 706.07(d).

CONCLUSION

Accordingly, it is believed that this application is now in condition for allowance and an early indication of its allowance is solicited. However, if the Examiner has any further matters that need to be resolved, a telephone call to the undersigned at 510-663-1100 would be appreciated.

Respectfully submitted,
Weaver Austin Villeneuve & Sampson LLP

/Peter Gallagher/

Peter A. Gallagher
Reg. No. 47,584

P.O. Box 70250
Oakland, CA 94612-0250
510-663-1100